Inventor: Wendell P. Noble

Title: Semiconductor Processing Methods of Forming Integrated Circuitry, Forming Conductive Lines, Forming a Conductive Grid, Forming a Conductive Network, Forming an Electrical Interconnection to a Node Location, Forming an Electrical Interconnection with a Transistor Source/Drain Region, and Integrated Circuitry

Assignee: Micron Technology, Inc.

INFORMATION DISCLOSURE STATEMENT

PURSUANT TO 37 C.F.R. §§ 1.56, 1.97 AND 1.98

In compliance with 37 C.F.R. §§ 1.56, 1.97 and 1.98, your attention is directed to the United States patents and other references listed on the attached Form PTO-1449. No admission is made regarding whether all the submitted references are prior art.

The listed references were cited by, or submitted to, the Office in the parent, co-pending application of the above-identified application. The above-identified application is a divisional application of co-pending application Serial No. 10/227,500, filed August 22, 2002. Such prior disclosure is sufficient for the above-identified application as far as copies of the references are concerned. 37 C.F.R. § 1.98(d) and MPEP § 609(2).

Citation of these references is respectfully requested.

Respectfully submitted,

Dated: 7/29/03

By: _____

Robert C. Hyta
Reg. No. 46,791

EV317134177

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. M122-2378	SERIAL NO. Filed Herewith
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)		APPLICANT Wendell P. Noble	
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U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,539,229	07/96	Noble, Jr., et al.			
	AB	5,214,603	05/93	Dhong, et al.			
	AC	4,604,162	08/86	Sobczak			
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							Yes	No
	AQ	0 720 221 A1	07/96	EPO				
	AR							
	AS							

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	AT		Davari et. al., "A Variable-Size Shallow Trench Isolation (STI) Technology With Diffused Sidewall Doping For Submicron CMOS,"
			IEDM Technical Digest, International Electron Devices Meeting, San Francisco, CA, Dec. 11-14, 1988, pp. 92-95.
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			1990 VLSI Technology Symposium, Honolulu, HI, June 4-7, 1990, pp. 11-12.

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,241,211	08/93	Tashiro			
	AB						
	AC						

FOREIGN PATENT DOCUMENTS

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							Yes	No
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	AS		Suma et. al., "An SOI-DRAM With Wide Operating Voltage Range by CMOS/SIMOX Technology," *IEEE Journal of Solid-State*
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			Vol. 39, Pub No. 6, June 1996.
			Takahiro Onai et al., "SEPIA: A New Isolation Structure for Soft-Error-Immune LSI's," 1993 IEEE, 3 pages.

EXAMINER	DATE CONSIDERED

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